WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a clock input terminal to which external clocks are supplied;

a PLL circuit, which is supplied with the external clocks and generate first internal clocks;

a logic circuit, which operates in synchronization with the internal clocks; and

an internal counter, which counts the first internal clocks when the PLL circuit is tested, wherein

the internal counter is provided with an output terminal from which an output signal thereof is supplied to an external circuit.

2. A semiconductor device according to claim 1, further comprising:

a control terminal to which a control signal is supplied from an external circuit when the test is started;

a first logic gate, which is supplied with the first internal clocks and the control signal; and

a reset terminal to which a reset signal is supplied from an external circuit to the counter, wherein

the counter operates in accordance with an output signal of the first logic gate and the reset signal.

3. A semiconductor device, comprising:

a clock input terminal to which external clocks are supplied;

a PLL circuit, which is supplied with the external clocks and generate first internal clocks;

a logic circuit, which operates in synchronization with the internal clocks;

a test clock terminal to which test clocks are supplied from an external circuit, the test clock having a frequency with a predetermined phase difference from the external clocks;

a flip-flop circuit, which is supplied with the test clocks and the first internal clocks to generate second internal clocks; and

an internal counter, which counts the second internal clocks when the PLL circuit is tested, wherein

the internal counter is provided with an output terminal from which an output signal thereof is supplied to an external circuit.

4. A semiconductor device according to claim 3, further comprising:

a second logic gate, which is supplied with the second internal clocks and the test clocks; and

a reset terminal to which a reset signal is supplied from an external circuit to the counter, wherein

the counter operates in accordance with an output signal of the second logic gate and the reset signal.

5. A semiconductor device, comprising:

a clock input terminal to which external clocks are supplied;

a PLL circuit, which is supplied with the external clocks and generate first internal clocks;

a logic circuit, which operates in synchronization with the internal clocks;

a test clock terminal to which test clocks are supplied from an external circuit, the test clock having a frequency with a predetermined phase difference from the external clocks;

a flip-flop circuit, which is supplied with the test clocks and the first internal clocks to generate second internal clocks;

an internal counter, which counts the second internal clocks when the PLL circuit is tested; and

a selector, which selectively transfer one of the first clocks and the second clocks to the counter, wherein

the internal counter is provided with an output terminal from which an output signal thereof is supplied to an external circuit.

6. A semiconductor device according to claim 5, further comprising:

a control terminal to which a control signal is supplied from an external circuit when a frequency test is started;

a first logic gate, which is supplied with the first internal clocks and the control signal; and

a reset terminal to which a reset signal is supplied from an external circuit to the counter, and

a second logic gate, which is supplied with the second internal clocks and the test clocks; wherein

the counter operates in accordance with an output signal of the selector and the reset signal.